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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,935	12/31/2003	Stanley S. Kulick	INTEL1	6672

6980 7590 01/18/2006

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EXAMINER	
IWASHKO, LEV	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 01/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,935	KULICK, STANLEY S.	
	Examiner	Art Unit	
	Lev I. Iwashko	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following are quotations of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an International application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-8, 10-13, 16-17, and 19-20 are rejected under U.S.C. 102(e) as being anticipated by Parrish et al. (US Patent 5,117,350)

Claim 1. A method, comprising: partitioning a computer memory *(Column 4, lines 65-67 – State that the memory can be partitioned)*

- into a freeable range and *(Column 11, lines 30-31 – Declare an external memory)*
- a non-freeable range of operating memory devices, *(Column 2, lines 50-55 – State that there is a main memory)*
- wherein pinned memory is confined to the non-freeable range and the operating memory devices in the freeable range constitute at least the same number of bytes as the operating memory devices in the non-

freeable range; *(Column 9, lines 15-25 – State that all the memory blocks are of the same byte size)*

- de-allocating at least a portion of the freeable range of memory devices; and *(Column 18, lines 21-24 – State that the partition table is updated with new information upon allocation)*
- copying the contents of the memory range supported by a memory device that holds pinned memory to at least one de-allocated memory device. *(Column 9, lines 15-25 – Describe how mapping the contents corresponds to size and pinned memory)*

Claim 2. The method of claim 1 further comprising re-routing requests destined for the memory device that holds pinned memory to the at least one de-allocated memory device when the contents of the memory range supported by the memory device that holds pinned memory are copied. *(Column 15, lines 21-26 – State that the write operation (re-routing) occurs when there is a request)*

Claim 3. The method of claim 1 further comprising re-partitioning the memory into a freeable range and a non-freeable range of operating memory devices when contents of the memory range supported by a memory device that holds pinned memory is copied. *(Column 17, lines 1-16 – Show how the proper information is written to either local or external blocks of memory partitions)*

Claim 4. The method of claim 1 further comprising interleaving the freeable range of operating memory devices when the computer memory is partitioned. *(Column 5, lines 7-10 – State that data can be duplicated (a.k.a. freeable range) for sharing after partitioning)*

Claim 5. The method of claim 1 further comprising interleaving the non-freeable range of operating memory devices when the computer memory is partitioned. *(Column 4, lines 58-64 – Describe how the memory may be partitioned to respond to input addresses)*

Claim 6. The method of claim 1 further comprising detecting whether an operating

memory device is failing when the failing memory device holds pinned memory; *(Column 18, lines 6-9 – State that the service call parameters are validated for being in the correct range)*

- de-allocating at least a portion of the freeable range of memory devices; and *(Column 18, lines 21-24 – State that the partition table is updated with new information upon allocation)*
- copying the contents of the memory range supported by the failing memory device to at least one de-allocated memory device. *(Column 18, lines 27-28 – State that the task is passed back to the address of the partition)*

Claim 7. The method of claim 6 wherein detecting whether an operating memory device is failing further comprises accepting at least one parameter indicative of a memory device failure based on a selected criterion for monitoring a memory device; *(Column 18, lines 6-9 – State that the service call parameters are validated for being in the correct range)*

- monitoring an operating memory device and generating monitoring data indicative of whether the memory device is in compliance with the selected criterion; *(Column 18, lines 10-12 – State the types of parameters that are reviewed)*
- and determining whether the selected criterion has been met. *(Column 18, lines 12-14 – State how an error message responds to the requesting task)*

Claim 8. The method of claim 7 wherein the selected criterion is a temperature threshold. *(Column 18, lines 7-9 – State that there is validation for being in the prescribed ranges)*

Claim 10. The method of claim 1 wherein de-allocating the freeable range of memory devices comprises issuing, by a software process, a de-allocation request, wherein the de-allocation request identifies the freeable range memory devices; *(Column 18, lines 6-28 – State that a "create memory partition" is requested)*

- receiving, at an operating system, the de-allocation request and determining whether the requested memory devices may be de-allocated; *(Column 18, lines 6-7 – State that a "create memory partition" is requested)*
- and issuing by an operating system process, a determination of whether the requested memory devices may be de-allocated. *(Column 18, lines 7-9 – State that there is a validation on whether or not the procedure may occur)*

Claim 11. The method of claim 1 wherein copying the contents of the memory range supported by a memory device that holds pinned memory to at least one de-allocated memory device further comprises selecting at least one de-allocated memory device suitable in size to replace the memory device that holds pinned memory, wherein the memory device that holds pinned memory is configured to contain a predetermined number of bytes of data. *(Column 9, lines 15-25 – Describe how mapping the contents corresponds to size and pinned memory)*

Claim 12. The method of claim 1 wherein copying the contents of the memory range supported by a memory device that holds pinned memory to at least one de-allocated memory device further comprises remapping an address location for the memory device that holds pinned memory to an address location for the at least one de-allocated memory device utilized for replacing the memory device that holds pinned memory. *(Column 9, lines 25-35 – Describe the remapping procedure)*

Claim 13. A method comprising:

- issuing, by the controller process, a partition call to *(Column 13, lines 21-25 – State that there is a controller that dynamically partitions the memory)*
- partition a computer memory *(Column 4, lines 65-67 – State that the memory can be partitioned)*

- into a freeable range and *(Column 11, lines 30-31 – Declare an external memory)*
- a non-freeable range of operating memory devices; *(Column 2, lines 50-55 – State that there is a main memory)*
- receiving, by the operating system process, the partition call and processing the call to partition the computer memory, wherein pinned memory is confined to the non-freeable range; issuing, by the controller process, a de-allocation call to de-allocate the freeable range of memory devices; receiving, by the operating system process, the de-allocation call and processing the call to de-allocate the freeable range of memory devices; and *(Column 18, lines 6-43 – Describe the "create memory partition" and "delete memory partition" requests)*
- issuing, by the operating system process, a copying call to copy the memory range supported by a memory device containing pinned memory to at least one de-allocated memory device. *(Column 18, lines 44-46 – State that there is an "attach memory partition" request)*

Claim 16. The method of claim 13 wherein the memory device containing pinned memory is failing. *(Column 10, lines 48-50 – Describe memory invalidation and dirty memory)*

Claim 17. The method of claim 13 wherein, collectively, the operating memory devices in the freeable range constitute at least the same number of bytes as the operating memory devices in the non-freeable range. *(Column 9, lines 15-25 – State that all the memory blocks are of the same byte size)*

Claim 19. A system comprising: *(Column 4, lines 65-67 – State that the memory can be partitioned)*

- a partitioning component operable to partition a memory *(Column 4, lines 65-67 – State that the memory can be partitioned)*
- into a freeable range and *(Column 11, lines 30-31 – Declare an external memory)*

- a non-freeable range of operating memory devices, *(Column 2, lines 50-55 – State that there is a main memory)*
- wherein pinned memory is confined to the non-freeable range; and *(Column 2, lines 50-55 – State that there is a main memory)*
- a memory controller operable to de-allocate the freeable range of memory devices and copy the memory range supported by a memory device which contains pinned memory to at least one de-allocated memory device. *(Column 1, lines 36-38 – Describe memory control logic)*

Claim 20. The system of claim 19, wherein the memory controller is further operable to copy the memory range supported by a memory device which contains pinned memory to at least one de-allocated memory device when the memory device which contains pinned memory is failing. *(Column 10, lines 51-54 – State that the control of partition RAM supports cache memory invalidation)*

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 9 is rejected under 35 U.S.C.103(a) as being unpatentable over Parrish et al. as applied to claims 1, 6, and 7 above, further in view of Savage et al. (US Patent 4,797,853).

Parrish teaches the limitations of claims 1, 6, and 7 for the reasons above.

Parrish 's invention differs from the claimed invention in that there is no specific reference to a threshold error rate.

Parrish fails to teach claim 9, which states: "The method of claim 7 wherein the selected criterion is a threshold error rate." However, Savage 's invention discloses an "error counter" (Column 23, line 46). It would have been obvious to one of ordinary skill in the art, having the teachings of the "Memory Address Mechanism" of Parrish and Savage 's "Direct Memory Access Controller" before him at the time the invention was made, to allow for there to exist a threshold error rate so that errors could be tracked and counted, thereby making sure that the system runs efficiently.

5. Claims 14 and 15 are rejected under 35 U.S.C.103(a) as being unpatentable over Parrish et al. as applied to claim 13 above, further in view of Bauman et al. (US Patent 6,415,364 B1).

Parrish teaches the limitations of claim 13 for the reasons above.

Parrish 's invention differs from the claimed invention in that there is no specific reference to an interleaving call.

Parrish fails to teach a portion of claims 14 and 15, which namely state: "The method of claim 13 further comprising issuing, by the controller process, an interleaving call to interleave the freeable/non-freeable range of operating memory devices; and receiving, by the operating system process, the interleaving call and processing the call to interleave the freeable/non-freeable range when the memory range supported by the memory device containing pinned memory is copied to at least one de-allocated memory device". However, Bauman 's invention discloses an "interleaving or requests" process" (Column 19, lines 57-67 and Column 20, lines 1-10). It would have been obvious to one of ordinary skill in the art, having the teachings of the "Memory Address Mechanism" of Parrish and Bauman 's "High Speed Memory Storage Unit" before him at the time the invention was made, to allow for there to be an

interleave call in order to make the system aware of the commands it was running, thereby maximizing efficiency.

6. Claim 18 is rejected under 35 U.S.C.103(a) as being unpatentable over Parrish et al. as applied to claim 13 above, further in view of Bauman et al. (US Patent 6,381,715 B1).

Parrish teaches the limitations of claim 13 for the reasons above.

Parrish 's invention differs from the claimed invention in that there is no specific reference to DIMMs.

Parrish fails to teach claim 18, which states: "The method of claim 13 wherein the memory devices are DIMMS." However, Bauman 's invention discloses that "each MSU expansion includes two Dual In-Line Memory Modules" (Column 10 lines 49-51). It would have been obvious to one of ordinary skill in the art, having the teachings of the "Memory Address Mechanism" of Parrish and Bauman 's "System and method for performing parallel initialization and testing of multiple memory banks and interfaces in a shared memory module" before him at the time the invention was made, to allow for the memory devices to be DIMMs so that memory space could be conserved, thereby increasing the speed and efficiency of the entire system.

7. Claims 21 and 22 are rejected under 35 U.S.C.103(a) as being unpatentable over Parrish et al. as applied to claim 19 above, further in view of Tsang (US Patent 5,537,112 A).

Parrish teaches the limitations of claim 19 for the reasons above.

Parrish 's invention differs from the claimed invention in that there is no specific reference to an interleaving component.

Parrish fails to teach a portion of claims 21 and 22, which namely state: "The system of claim 19 further comprising an interleaving component operable to interleave the freeable/non-freeable range of operating memory devices when the memory range supported by the memory device which contains pinned memory is copied to at least one de-allocated memory device." However, Tsang 's invention discloses an "interleaving device for interleaving the bits of each corresponding second group with the selected number of ordered bits of binary data of each corresponding word to obtain the corresponding codewords" (Abstract, lines 13-16). It would have been obvious to one of ordinary skill in the art, having the teachings of the "Memory Address Mechanism" of Parrish and Tsang 's "Method and apparatus for implementing run length limited codes in partial response channels" before him at the time the invention was made, to allow for there to be an interleaving component so that an entire device could take care of the interleaving aspect of the system, thereby maximizing the system's efficiency (due to task delegation).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lev I. Iwashko whose telephone number is (571)272-1658. The examiner can normally be reached on M-F (alternating Fridays), from 8-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lev Iwashko

MATTHEW D. ANDERSON
PRIMARY EXAMINER